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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/927,545	08/09/2001	Peter Schlemm	A-2812	6082
24131 7590 07/17/2007 LERNER GREENBERG STEMER LLP P O BOX 2480 HOLLYWOOD, FL 33022-2480			EXAMINER GUTIERREZ, ANTHONY	
			ART UNIT 2857	PAPER NUMBER
			MAIL DATE 07/17/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

09/927,545

Applicant(s)

SCHLEMM, PETER

Examiner

Anthony Gutierrez

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 April 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 July 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date. _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohwada (U.S. Patent No. 4,443,849) in view of Lytel et al. (U.S. Patent No. 5,039,189).

As to claims 1, 6, and 9, Ohwada discloses a method of executing method steps with an apparatus, with the method comprising: enabling the apparatus for switching an error mode on or off via an input (the apparatus starts in a normal mode and switches to an error mode when an error takes place in one of the package units, thus switching the error mode on. The switching is done via an input (See Fig.2 as the error detecting circuits 46, 47, 48 check package units 41, 42, 43, and detect that an error in one of the packages takes place via an input from the package into the respective error detecting circuit)) and checking whether an error mode is switched on via the input (col. 4, lines 23-29, col. 5, line 58-col. 6, line 5 and col. 4, lines 47-52); and producing an output signal in a method step and outputting the output signal only if the error mode is switched on (col. 7, lines 43-51). The error signal ER is only produced and sent out when an error is detected. An error mode is switched on only when an

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error is detected. Therefore if the error mode is not switched on, it will be because no error has been detected, and thus there will be no output signal to output.

While Ohwada discloses that the invention relates to an error recovery system for use in an electronic digital computer system comprising a plurality of processors (col. 1, lines 9-11), Ohwada does not specifically teach that the output signal is output as at least one of an optical or acoustic signal.

Lytel et al., however, teaches a method for converting electrical signals into optical signals (col. 1, lines 7-11). Lytel et al. also teaches that existing microelectronics can produce high-speed integrated circuits that are capable of operating at high frequencies (col. 1, lines 15-17). Lytel further teaches that converting electrical signals into optical signals provides numerous benefits (col. 2, lines 3-12).

It therefore would have been obvious to one of ordinary skill in the art at the time of invention to implement the signal transmissions between processors disclosed by Ohwada, through optical signals as taught by Lytel et al. in order to lower noise, propagation delay, power dissipation, and increase packing density, so that the speed of processing can be reliably increased.

As to claims 2-5, and 10-13, Ohwada further discloses wherein the method steps are divided into modules, and the method comprises changing from one module to another module during the execution of the method steps, and wherein the output signal comprises an identifier indicating in which module the output signal was produced (col. 5, lines 8-15 and col. 12, lines 44-51).

As to claims 7, 8, 14, and 15, Ohwada further discloses wherein the output signal is stored in a storage device, together with an indication of a time at which the output signal was stored (col. 7, line 58-col. 8, line 11).

As to claim 16, Ohwada further discloses input means configured to enable selective switching on and switching off of the error mode even during the execution of the method steps (col. 6, lines 40-50).

Response to Arguments

3. Applicant's arguments filed 4/25/07 have been fully considered but they are not persuasive.

Applicant has amended the claims to include the feature that the error mode is switched on or off via an input.

The Examiner addressed in the previous Officer Action rejection that Ohwada discloses that the error mode is switched on when an error occurs in one of the package units. An error detecting circuit is used to determine that an error occurred in one of the packages, the error mode thus being switched on.

Since this is detected by the detecting circuit via an input into the detecting circuit from the package unit, the Examiner maintains that the switching on of the error mode is done via an input.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a):

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony Gutierrez whose telephone number is (571) 272-2215. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eliseo Ramos-Feliciano can be reached on (571) 272-7925. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AG 7/6/07
Anthony Gutierrez

Art Unit 2857

7/6/07

Hal Wachon
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PRIMARY EXAMINER
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